6.7 GHz FREQUENCY SYNTHESIZER IN 0.8 μm SILICON BIPOLAR PRODUCTION TECHNOLOGY

STUDENT PAPER

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Abstract **This paper presents a 6.7 GHz phase-locked loop frequency synthesizer in a low-cost 0.8 μm/25 GHz-f_T silicon bipolar production technology. The total power consumption of 82 mW @ 3 V includes the power consumption of the voltage-controlled oscillator, the phase-frequency detector, the charge pump, the loop filter, and the divider. The synthesizer offers a phase noise performance of -103 dBc/Hz @ 1 MHz offset from the carrier. 6.7 GHz is the highest operating frequency for silicon-based synthesizers published.**

I. Introduction

The demand for low-cost wireless applications will increase rapidly within the next few years. High volume products, for example applications for wireless local area networks (WLANs) like Bluetooth at 2.4 GHz, and HIPERLAN at 5.2 GHz are strongly dependent on the availability of low-cost integrated circuits. Integrated frequency synthesizers in phase-locked loop (PLL) architecture are key components in all these wireless systems. They have voltage-controlled oscillators (VCOs), dividers, and phase detectors (PDs) on chip. On the highest level of integration the loop filter (LPF) is also implemented on chip. During the last years highly-integrated PLL-synthesizers with output frequencies up to 5.2 GHz have been published in CMOS ([1], [2], [3], [4], [5]), Si bipolar ([6], [7]), Si BiCMOS ([8]), and SiGe BiCMOS ([9]) technologies. Multi-GHz applications are supported with frequency synthesizers using GaAs-HEMT technology (e.g. [10]).

This work presents a frequency synthesizer in phase-locked loop architecture, fabricated in a silicon bipolar production technology, using conventional 0.8 μm-lithography. To our knowledge the operating frequency of 6.7 GHz is the highest reported for silicon-based frequency synthesizers up to date.

II. Technology

The frequency synthesizer was fabricated in Infineons B6HF Si bipolar production technology [11]. This 0.8 μm double-polysilicon technology uses simple LOCOS isolation, and features npn transistors with f_T = 25 GHz, lateral pnp transistors, three types of poly-Si resistors, linear MOS capacitors and ESD structures. Three metallization layers are available. Fig. 1 shows the cross section of a transistor with one base contact.

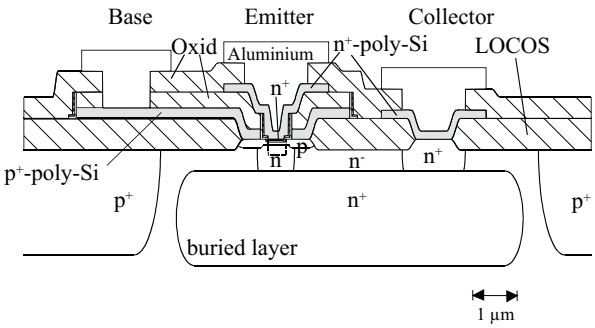

Fig. 1. Cross section of a 0.8 μm transistor.

III. Circuit Design

The PLL consists of the VCO, the divide-by-1024 circuit, and the phase-frequency detector (PFD) with charge pump (CP) output. There is only one external component, the loop filter. Thus single-loop (fig. 2) and multi-loop concepts (fig. 3) can easily be realized [12], [6].

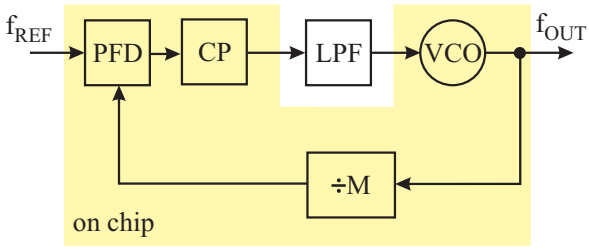

Fig. 2. Block diagram of single-loop concept.

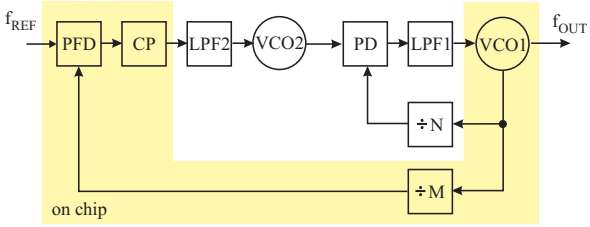

Fig. 3. Block diagram of a dual-loop concept.

All blocks were designed in fully differential logic. Fig. 4 shows the VCO topology. The oscillator consists of a cross-coupled differential amplifier with a resonant LC circuit acting as load. Emitter followers in the feedback path help to reduce the loading of the resonant circuits by the input of the differential amplifier and help to achieve a high loaded Q of the resonator. On-chip spiral inductors with inductances of 1.2 nH and transistors, used as varactors, build the resonant circuits. A course tuning of the output frequency of the oscillator can be performed by varying the operating current I_{CORE} of the oscillator [13].

The divide-by-1024 circuit consists of 10 T-type flip-flops with emitter followers for level shifting. The current of each flip-flop is matched to its frequency of operation. Fig. 5 shows the T-type flip-flop in master-slave configuration.

The structures of the PFD, the charge pump, and the passive loop filter are shown in fig. 6. The PFD

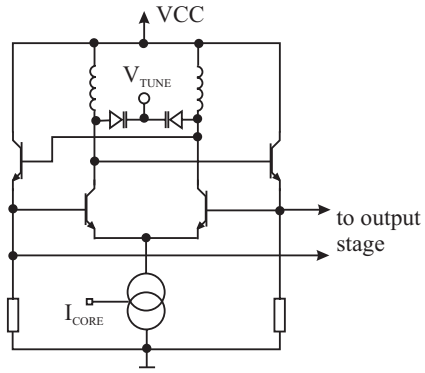

Fig. 4. Simple VCO circuit diagram.

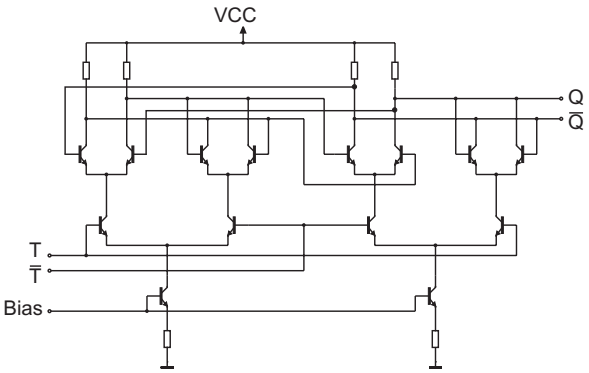

Fig. 5. T-type flip-flop.

consists of two resetable D-type flip-flops and a NAND-gate. The charge pump is realized by two current sources which are switched by the UP and DN signals of the PFD, dependent on the phase error between the reference signal and the divided-by-M output signal [12]. The passive loop filter is a RC network. C_2 helps to suppress spurious signals from the reference source.

IV. Experimental Results

All measurements were performed with PLL-chips mounted on printed circuit boards with supply voltage of 3 V. The high-frequency substrate had a thickness of 0.51 mm and ϵ_r of 3.38.

The total power consumption of 82 mW @ 3 V includes the power consumptions of the VCO, the PFD with charge pump, the divider, and the external loop filter. The PLL operates in the output frequency range from 6.4 GHz to 6.75 GHz with output power of -7.5 dBm.

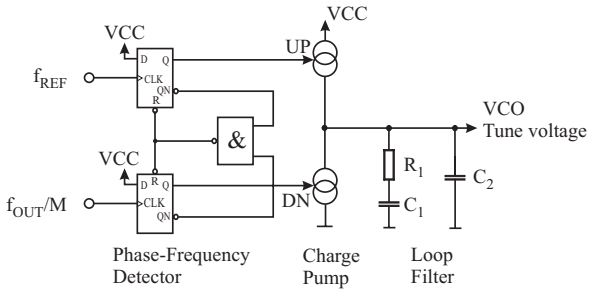

Fig. 6. Structures of the PFD, the charge pump, and the passive loop filter.

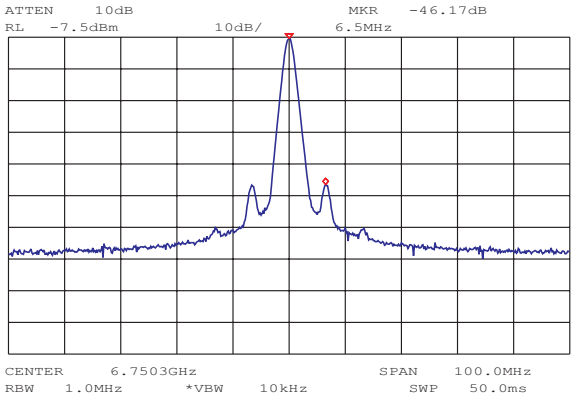

Fig. 7. Spectrum of the PLL output signal at 6.75 GHz in locked condition.

The spectrum of the output signal at 6.75 GHz in locked condition is presented in fig. 7. All spurious signals are 46 dB below the carrier at the maximum operating frequency.

The single-sideband (SSB) phase noise measurement results are shown in fig. 8 for locked and for free-running conditions at the output frequency of 6 GHz, due to the limited frequency coverage of the phase noise measurement equipment. This reduction of the output frequency was performed by increasing I_{CORE} of the VCO. The locked PLLs offer a phase noise performance of -103 dBc/Hz @ 1 MHz offset from the 6 GHz carrier. At frequency offsets smaller than the loop bandwidth, the phase noise is mainly determined by the phase noise of the PFD, the feedback divider, and the reference source. The measurements in free-running conditions were performed with identical VCOs on separate test boards.

The loop bandwidth was chosen to be 20 kHz and the damping factor ξ to be 0.85. The settling time for

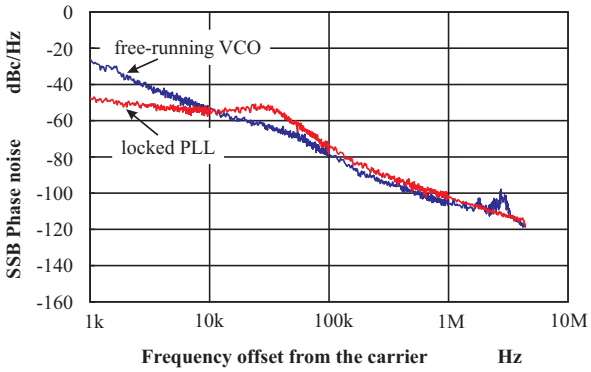

Fig. 8. Phase-noise performance in the locked and the free-running state at 6 GHz.

an output frequency step from 6.7 GHz to 6.55 GHz is approximately 150 μs and is shown in fig. 9.

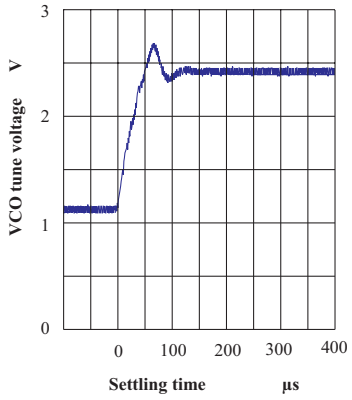

Fig. 9. Settling time of the PLL for an output frequency step from 6.70 GHz to 6.55 GHz.

The maximum output frequency of the VCO is 6.75 GHz and the tuning range (Fig. 10) is 350 MHz for tuning voltages from 0 V to 3 V at a supply voltage of 3 V.

The chip photograph is shown in fig.11. Table I sums up the technical data of the phase-locked loop.

V. Conclusions

A 6.7 GHz phase-locked loop frequency synthesizer in an 0.8 μm/25 GHz-f_T silicon bipolar production technology has been presented. The synthesizer offers tuning range of 350 MHz, phase noise performance of -103 dBc/Hz @ 1 MHz offset at the total power consumption of 82 mW @ 3 V. To our knowledge 6.7 GHz

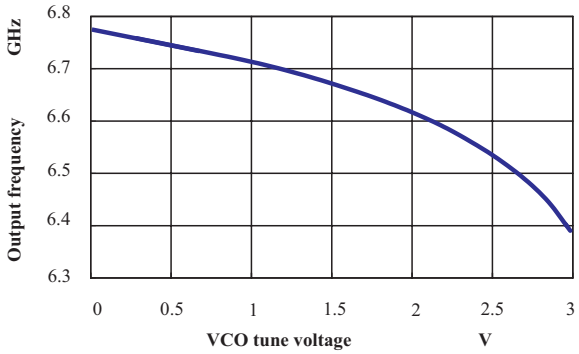

Fig. 10. Tune characteristic of the VCO.

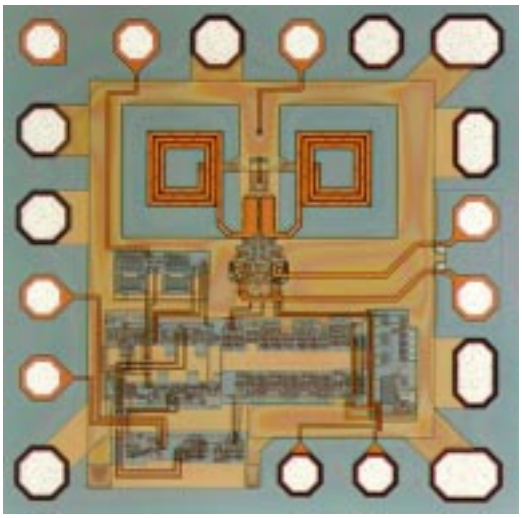

Fig. 11. Chip photograph (size: 776 μm x 776 μm).

is the highest reported operating frequency of synthesizers in silicon-based technologies.

TABLE I. Technical data.

Technology	0.8 μm-25 GHz-f_T Si bipolar (B6HF)
Power consumption	82 mW @ 3 V
Output frequency range	6.4 GHz - 6.75 GHz
Output power	-7.5 dBm
SSB-Phase noise	-103 dBc/Hz @ 1 MHz
Spurious suppression	46 dB @ 6.75 GHz
Chipsize	0.776 x 0.776 mm^2

References

[1] J. F. Parker, D. Ray, "A 1.6-GHz CMOS PLL with On-Chip Loop Filter," *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 3, pp. 337-343, 1998.

[2] J. Craninckx, M. S. J. Steyaert, "A Fully Integrated CMOS DCS-1800 Frequency Synthesizer," *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 12, pp. 2054-2065, 1998.

[3] M. H. Perrott, T. L. Tewksbury III, C. G. Sodini, "A 27-mW CMOS Fractional-N Synthesizer Using Digital Compensation for 2.5-Mb/s GFSK Modulation," *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 12, pp. 2048-2060, 1997.

[4] C. Lam, B. Razavi, "A 2.6-GHz/5.2-GHz Frequency Synthesizer in 0.4-μm CMOS Technology," *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, pp. 117-120, 1999.

[5] H. R. Rategh, H. Samavati, T. H. Lee, "A 5GHz, 32mW CMOS Frequency Synthesizer With an Injection Locked Frequency Divider," *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, pp. 113-116, 1999.

[6] A. N. Hafez, M. I. Elmasry, "A Fully-Integrated Low Phase-Noise Nested-Loop PLL for Frequency Synthesis," *IEEE Proceedings of the Custom Integrated Circuits Conference 2000*, pp.589-592, 2000.

[7] W.-Z. Chen, J.-T. Wu, "A 2-V, 1.8-GHz BJT Phase-Locked Loop," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 6, pp. 784-789, 1999.

[8] T. S. Aytur, B. Razavi, "A 2-GHz, 6-mW BiCMOS Frequency Sythesizer," *IEEE Journal of Solid-State Circuits*, Vol. 30, No. 12, pp. 1457-1462, 1995.

[9] H. Ainspan, M. Soyuer, "A Fully-Integrated 5-GHz Frequency Synthesizer in SiGe BiCMOS," *IEEE Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting 1999*, pp. 165-168, 1999.

[10] W. Baumberger, M. Lang, P. Leber, M. Rieger, W. Bronner, A. Huelsmann, K. Koehler, "A Completely Integrated One-Chip 18 GHz Frequency Synthesizer Using HEMT-Technology," *IEEE Proceedings of the European Solid-State Circuits Conference ESSCIRC96*, pp. 360 - 363, 1996.

[11] H. Klose, R. Lachner, K. Schön, R. Mahnkopf, K. Malek, M. Kerber, H. Braun, A. v. Felde, J. Popp, O. Cohrs, E. Bertagnolli, P. Sehring, "B6HF: A 0.8 micron 25 GHz/25 ps bipolar technology for "Mobile Radio" and "Ultra Fast Data Link" IC-products," *IEEE Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting 1993*, pp. 125-127, 1993.

[12] U. L. Rohde, *Digital PLL Frequency Synthesizers*, Prentice Hall Inc. N.J., 1983.

[13] H. Knapp, H.-D. Wohlmuth, J. Böck, A. Scholtz, "22 GHz monolithically integrated oscillator in silicon bipolar technology," *Electronics Letters*, Vol. 35, No. 6, pp. 438-439, 1999.